Channel and Pin Assignment for Three Dimensional Packaging Routing

Jacob Minz and Sung Kyu Lim
School of Electrical and Computer Engineering
Georgia Institute of Technology
{jrminz,limsk}@ece.gatech.edu

***Abstract*— Three dimensional packaging is becoming a popular concept because of the numerous advantages it has to offer over the existing conventional technologies such as PCB and MCM. System on Packages (SOP) is an example of three dimensional packaging. In this paper, we present the channel and pin assignment algorithms for 3D packaging routing. There exist multiple floorplan, routing, and pin distribution layers in SOP. The purpose of SOP channel assignment is to finish the connection between a pair of floorplan and pin distribution layers. We perform SOP pin assignment in case the pin location of some blocks in floorplan layer is not known. Our related experimental results demonstrate the effectiveness of our algorithm.**

I. Introduction

The true potential of SOP (System-On-Package) technology [1] lies in its capability to integrate both mixed-signal active components and passive components all into a single high speed/density three dimensional packaging substrate as illustrated in Figure 1. Innovative ideas in the development of computer-aided design (CAD) tools for multi-layer SOP technology is crucial to fully exploit the potential of this new emerging technology. However, there has been very little development, if not none, of CAD tools that handle the complexity of automatic 3D SOP layout generation. The physical layout resource of SOP is multi-layer in nature: all layers are used for both placement and routing, and pins are now located at all layers. Therefore, the existing design tools for PCB or MCM packaging can not be used directly for the design of SOP. Therefore, our primary goal is to make the best use of placement and routing layers available while automatically generating 3D package layout under various noise constraints.

In this paper, we present the channel and pin assignment algorithms for 3D packaging routing. There exist multiple floorplan, routing, and pin distribution layers in SOP. The purpose of SOP channel assignment is to finish the connection between a pair of floorplan and pin distribution layers. We perform pin assignment in case the pin location of some blocks in floorplan layer is not known. Our related experimental results demonstrate the effectiveness of our algorithm. We also review various approaches for the PCB, IC and MCM routing algorithms and investigate their applicability to the SOP model. This work completes our recently proposed global routing flow [2], [3] for 3D packaging.

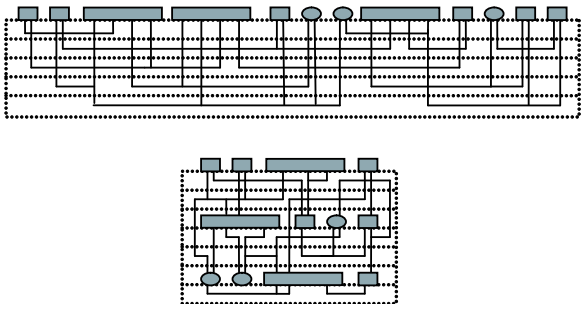

Fig. 1. Single active layer (PCB,MCM) vs multiple active layer (SOP) packaging

II. Preliminaries

A. MCM vs SOP Routing

The routing problem for MCM is different from PCB or IC primarily due to the large number of layers available in MCM. A typical MCM has upto 60 signal layers as compared to 4 in PCB or 8 in IC. Not only the routing was to be done in each layers, but now the inter-layer constraints needed to be handled as well. The inter-layer connection was done by means of via. The major design criteria was performance. Performance is affected by such factors as crosstalk, delay and manufacturability constraints. MCM routing is a multi-layer, multi-objective optimization problem. Some of the objectives include wirelength, via, crosstalk, layer minimization under manufacturability constraints. Most of the initial work on MCM routing considered wirelength only. Maze routing was extended for MCM [4]. This simple but powerful algorithm has serious drawbacks in that it is a sequential routing algorithms and has high memory requirements.

In general, MCM routing is done in multiple phase: pin redistribution, layer assignment and detailed assignment. The problem of layer assignment is proven to be NP-complete. Some works have considered an integrated pin redistribution and routing approach such as SLICE [5] and V4R [6]. The unique feature for V4R is that it uses only 4 vias for every 2 pin nets and $4(k-1)$ for each k-terminal net. These routers handle routing layer and via minimization quite efficiently. Most MCM routers use grid-based approach, which suffers from memory requirements for dense designs. SURF [7] is a gridless MCM router based on rubber-band sketches.

Performance-driven routing for MCM involves generating routing topology for nets in a coarse grid. The topology optimization typically depend on some delay models [8]. A huge volume of works can be found in the literature that deal with delay minimization for single nets [9]. A layer assignment for crosstalk minimization is done in [10].

A notable difference between SOP and MCM routing lies in the fact that there exists *multiple* placement layers in SOP, whereas in MCM there is only one placement layer. Therefore, nets are now connecting pins located in *all* intermediate layers in SOP. In MCM, however, all pins are located *only* at the top layer. This makes SOP or 3D package routing problem more general than MCM routing. In this paper, we present the design of a complete global router for 3D packages, which to the best of our knowledge is the first one reported in the literature. The main goal is to decompose the 3D problem into a set of 2D problems so that we are able to use existing 2D algorithms to solve the 3D problem effectively. We show in this paper that the way we decompose the 3D problem has a huge impact not only on various design objectives such as wirelength, via, layer but also on the complexity of 2D sub-problems and the runtime needed to solve them.

B. Problem Formulation

The layer structure in SOP is different from PCB or MCM– it has multiple floorplan layers and routing layers. It has one *I/O pin layer* through which various components can be connected to the external pins. The *floorplan layers* contain the blocks (such as ICs, embedded passives, opto-electric components, etc), which from the point of view of physical design is just a geometrical object with pins. The interval between two floorplan layers is called the *routing interval*. The routing interval contains a stack of *signal routing layers* sandwiched between *pin distribution layers*. These layers are actually X-Y routing layer pairs, so that the rectilinear partial net topologies may be assigned to it. We also allow routing to be done in the pin distribution layers.

In the SOP model the nets are classified into two categories. The nets which have all their terminals in the same floorplan layer are called *i-nets*, while the ones having terminal in different floorplan layers are *x-nets*. The i-nets can be routed in the single routing interval or indeed within the floorplan layer itself. However, for high performance designs routing such nets in the routing interval immediately above or below the floorplan layer maybe desirable and even required. On the other hand, the x-nets may span more than one routing intervals.

We define the SOP global routing problem formally as follows:

Definition 1 (SOP Global Routing): Given a set of floorplans F and netlist N, generate a routing topology for each net n, assign n to a set of routing layers and assign all pins of n to legal locations. All conflicting nets are assigned to different routing layers while satisfying various capacity constraints. The objective is to minimize the total number of routing layers used, wirelength, and crosstalk.

We need to perform *Channel Assignment* to finish the connection between pin distribution layer and floorplan layer. The formal definition of channel assignment problem is as follows:

Definition 2 (SOP Channel Assignment): Given a set of pins P from a pin distribution layer and a set of channels C from a floorplan layer, we find an assignment $P \rightarrow C$ such that wirelength, number of layers, and number of bends are minimized while channel capacities are not violated.

In case some blocks are a collection of cells (= soft blocks), the pins may not be assigned and *Pin Assignment* needs to be done to determine their exact location along the boundary. The formal definition of pin assignment problem is as follows:

Definition 3 (SOP Pin Assignment): Given a set of blocks B, a set of channels C, and a set of nets N connecting a pair of block and channel, find location of pins along the boundary of each block such that wirelength, maximum pin demand, and maximum routing demand are minimized.

Pin demand is the number of nets using the same block boundary, and routing demand is the number of nets using the same routing region. Both objectives have a direct relation to congestion in 3D structure of SOP.

III. SOP Global Routing Algorithm

In this section, we first provide an overview of our 3D global routing algorithm. We then present the summary of our recent work on pin/net distribution and 2D layer assignment. Lastly, we present our channel assignment and pin assignment algorithms.

A. Overview of 3D Global Routing

Our 3D router, illustrated in Figure 2, is divided into the following steps: (1) coarse pin distribution, (2) net distribution, (3) detailed pin distribution, (4) topology generation, (5) 2D layer assignment, (6) channel assignment, and (7) pin assignment step. The main purpose of our multi-step effort is to divide the 3D problem into a set of 2D problems so that we are able to use existing 2D algorithms to solve the 3D problem effectively. The process of determining the location of entry/exit points for each routing interval is called pin distribution. The process of assigning nets to routing intervals (= routing layers between a pair of floorplan layers) is called net distribution step. In the coarse pin distribution step, which is done before net distribution, we find a coarse location for the pins and use this information for the net distribution. After the net distribution, detailed pin distribution step assigns finer location to all pins. A Steiner tree based routing topology for each net is constructed and a layer pair is assigned to it during topology generation step. In case we have many nets, the conflict among the nets for routing resources is resolved and layer pairs are assigned during 2D layer assignment step. The channel assignment problem is to assign each pin in the pin distribution layers to a channel in the floorplan layers. The purpose of pin assignment is to assign a location to the pin on the block boundary in a floorplan layer.

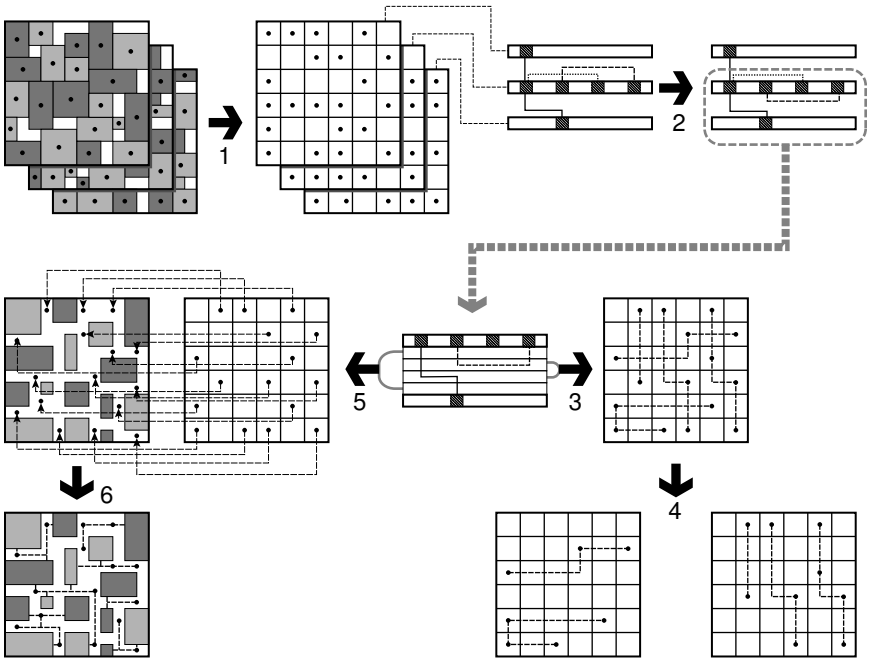

Fig. 2. Overview of the global routing process. 1=pin distribution, 2=net distribution, 3=topology generation, 4=layer assignment, 5=channel assignment, 6=pin assignment.

B. Summary of Our Recent Work

We recently have implemented the Coarse Pin Distribution and 2-D Layer Assignment [2] and Net and Pin Distribution [3] for 3D packaging layout. For topology generation, we have used an existing RSA/G heuristic [11] to generate the net topologies at each routing interval since the minimum arborescence is a good representative for the topology of a net in a high performance design. We summarize our algorithms here:

- Coarse Pin Distribution: We generate coarse locations for all pins of the nets in the routing interval. For the purpose of pin distribution we flatten the 3-D SOP structure to 2-D and superimpose a $A \times B$ grid on it. We use our partitioning algorithm [12] to evenly distribute pins to all the partitions formed by this grid while keeping the wirelength minimum. This partitioning algorithm is modified so that it does not move the pins far from their initial locations.
- 2-D Layer Assignment: We construct a Layer Constraint Graph (LCG) from the given global routing topology, where each node represents a net and two nodes in the LCG have an edge between them if corresponding net segments of same orientation (horizontal or vertical) share at least one tile in the routing grid. We use a fast node coloring heuristic algorithm to assign a color to the node such that no two nodes sharing an edge are assigned the same color.
- Net Distribution: The net distribution problem is modeled as a graph with each i-net in the routing interval as node and the crosstalk interaction as edges. The coarse pin distribution is used as the approximate location of the pins. The problem can then be seen as a restricted graph partitioning problem where some of the nodes can only go to one of two pre-determined partitions.
- Detailed Pin Distribution: We legalize the location of the pins while respecting the coarse pin assignment and optimizing wirelength. The results of the coarse pin assignment are used for force-directed placement of the pins in the pin distribution layers. The pins in each routing interval are sorted according to their weights. The pins are then sequentially assigned to grids previously determined.

C. SOP Channel Assignment Algorithm

The pins in the routing interval have to be connected to their corresponding blocks in the floorplan layer. The pins are connected to the floorplan layer using vias which can only be accommodated in the routing channels. The pins therefore have to be assigned a channel in the floorplan layer. The channel assignment of pins will affect the additional number of layers and total wirelength. Since one desirable objective is to reduce the number of bends (which would necessitate the use of secondary vias), we assume a straight or L-shaped routing of nets to their assigned channel. This reasonable assumption simplifies the evaluation of the wirelength. We observed that congestion of pin connections and wire crossings on a particular channel would increase the layer count. Our cost model for the problem captures these issues and our algorithm minimizing the cost function, assigns every pin to a channel. For this problem we are given the location of the pins and the location, length, orientation (horizontal or vertical)

```
=========================================
Algorithm: CHNL_DIST
Input: pins, channels
Output: channel assignment & num. of layers
-----------------------------------------
Determine via capacities for each channel
For all pins
  Find a channel with min. assignment cost
    and  not violating the constraints.
  Calculate channel crossings.
  Update via and routing demands.
  Assign this channel to the pin.
Calculate and report number of layers.
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Fig. 3. SOP channel assignment algorithm

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=========================================
Algorithm: 2PIN_ASSIGN
Input: 2-D floorplan, netlist
Output: routes and course pin assignment
-----------------------------------------
Generate FCG from the floorplan.
Generate 2-pin subnets  for all nets.
Initialize the dynamic cost of the edges.
For all 2-pin subnets
  Find shortest path.
  Update the cost of edges of the path.
Rip-up and reroute in constraint version.
=========================================
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Fig. 4. SOP pin assignment algorithm

and via capacities of the channel. We seek to minimize the additional number of layers and wirelength while assigning every pin to a channel.

We derive the number of layers as follows. We assume that the channels will only accommodate rectilinear routes perpendicular to their orientation. For example, only vertical routes can terminate at or cross horizontal channels. This is a reasonable assumption because routes can still go in parallel over that channel; however they terminate at some other channels. We note that both terminating and crossing routes on the channel affects the routing demands on the channel. The routing demands were classified into left (top) or right (bottom) demands for vertical (horizontal) channels. Let the maximum of the two routing demands divided by the channel capacity be the density. Then the number of layers for the channel assignment is given by the maximum density among all channels.

The algorithm (Figure 3) for channel assignment assigns channels to the pins based on the costs of channel assignment. The cost is the sum of L-distance between pin and channel, the channel density and the bending penalty, multiplied by constants to reflect the relative importance. However, the constants are finalized by trying different values for a particular benchmark and finalizing it for all experiments. The L-distance and bending penalty between channel and pin is constant part of the cost while the channel density needed to be updated with an assignment.

The algorithms starts by estimating the via capacities of each channels. As an aside, in the case of MCMs the pins from the chip layers are fixed. In order that the channel assignment be legal, the via capacities of each channel should not be exceeded. A legal channel assignment can be got by following a sequential approach. The pins are assigned the channel greedily. The channel assignment for a pin involves search of the best cost channels. This is done efficiently by maintaining two ordered lists of horizontal and vertical channels and only examining the channels which are in the neighborhood of the pins. In order to estimate layers, channel crossings are determined. The assignment of a pin to a channel results in the change of the via counts and routing demands. This changes effect future channel assignments for other pins. However since the pins have been distributed evenly in a particular interval, sequential approach with no particular ordering of the pins does not degrade solution quality that much.

D. SOP Pin Assignment Algorithm

The final step in our proposed methodology connects the nets to its original terminals. The pin assignment is done entirely in the floorplan layer. Since the connections of the nets are specified by a set of blocks, the location of the terminals on the block boundary is to be determined. The routing channel is used to finish the last connections from the channel pins (determined during channel assignment) to the block. The channel pins are actually the entry/exit points to the routing interval. An interesting aspect of this problem is that complete connections of the blocks and channel pins of a net is not necessary since the channel pins of a net are connected in the routing interval. Hence it suffices if the block is connected to at least one channel pin. This observation reduces the problem to a 2-terminal net pin assignment. We model the floorplan with a Floorplan Connection Graph. The pin is now either a block node or channel node. We use modified Dijkstra's algorithm to find the most feasible coarse location for the terminals on the block boundary.

The pseudocode is given in Figure 4. The key to efficiently do pin-assignment for 3-D packaging is to have a good 2-pin net generation. The pins which had been projected to routing intervals during pin generation for routing interval now needs to be connected to its originating blocks. However, the pins can also connect to blocks closer to them, which form the part of the same net, if the costs are improved. The edge weights of the FCG derived from the floorplan are initialized. In the proposed solution we try to minimize the demands on routing as well as the pin-assignment edges while determining the path between the source and destination nodes. We force selection of different routes by making the costs of the edges in the path high. This ensures fair usage of resources modeled by the edges.

The algorithm operates on the FCG. For all nets connecting to the floorplan, 2-pin subnets are generated. The dynamic cost of the edges in FCG is initialized. For most subnets one end corresponds to the channel and other to the block. A shortest path is found between the subnets using the existing edge

TABLE I

BENCHMARK CHARACTERISTICS FOR GSRC SUITE AND OUR NEW GT SUITE

ckt	blks	nets	i-nets	x-nets
n10	10	118	31	87
n30	30	349	97	252
n50	50	485	76	409
n100	100	885	189	696
n200	200	1585	297	1288
n300	300	1893	339	1554
gt50	50	9419	2102	7317
gt100	100	16184	4361	11823
gt300	300	20072	4534	15538
gt1000	1000	32469	6908	25561
gt1500	1500	34725	6554	28171

weights. After the path is determined for a particular sub-net the weights of the edges are updated. The dynamic component of the weights are the demands. In order to ensure fair usage of the edges, all edges are penalized. This algorithm is also sequential and depends on the net-ordering.

IV. EXPERIMENTAL RESULTS

We implemented our algorithm GROUTE in C++/STL and ran experiments on a Dell Dimension 8800 Linux box. Our test cases are generated using our multi-layer SOP floorplanner [13] on GSRC benchmark circuits [14] and our own synthesized circuits, hereby called gt circuits. The gt circuits were synthesized by partitioning the IBM gate-level netlists [15]. These partitioned circuits were then used as inputs to the multilayer floorplanner. We fixed the number of layers to four. Benchmark characteristics are shown in Table I. The motivation of synthesizing our own benchmark was to test the algorithms on bigger and denser circuits. As shown in Table I, the gt circuits are denser than the GSRC ckts of same block sizes. Our layer usage results are based on the tile density $w = 10$. The RSA/G-based global routing trees are generated based on 10×10 unless otherwise specified. We ran our algorithms for channel assignment and pin assignment on GSRC and gt benchmarks and measured its solution quality as the values obtained for the various objectives. For our initial experiments, we have not taken the I/O layer into consideration.

A. Channel Assignment Results

We present the results of our Channel Assignment algorithm in Table II. In order to compare the quality of the solutions achieved by our channel assignment algorithm, we computed the best possible wirelength for a channel assignment, where via capacity violations were allowed. We tabulate the results of this scheme under the best wirelength. We compare the results of our algorithm with the best wirelength results for the number of layer pairs, wirelength, bends and number of pins violating channel via capacities. Our observation based on GSRC circuits is as follows:

- In channel assignment, we are close to the number of layers predicted by the best case. The increase in layers is due to increased routing density on the channels. The ratios of actual wirelength with best wirelength increase with the size of benchmarks.
- The violations in the best case and the number of bends reported by our algorithm are very close, suggesting that violations were fixed by bending the interconnections.

TABLE II

RESULT OF OUR CHANNEL ASSIGNMENT ALGORITHM. NUMBER OF LAYER PAIRS (LY), WIRELENGTH (WL), BENDS (BND) AND VIOLATIONS (VL) FOR THE BEST AND ACTUAL CASES ARE REPORTED. RUNTIME IS IN SECONDS.

	best wirelength				CHN_ASSIGN			
ckts	ly	wl	bnd	vl	ly	wl	bnd	vl
n10	5	6.9	0	55	5	14.1	34	0
n30	6	11.3	0	144	6	24.7	122	0
n50	6	14.8	3	282	6	32.0	189	0
n100	6	16.4	3	413	7	36.3	382	0
n200	6	24.1	1	845	8	61.4	917	0
n300	6	28.4	3	1000	8	65.1	1029	0
gt50	14	2.3	1062	8026	12	10.5	13113	0
gt100	13	3.2	1162	14151	15	18.7	22561	0
gt300	23	3.2	1038	19211	20	4.7	6385	0
gt1000	44	5.6	2444	37918	38	48.70	79745	0
gt1500	40	5.0	2509	41237	52	54.5	89256	0
TIME	1000				1300			

TABLE III

PIN ASSIGNMENT RESULTS, WHERE WIRELENGTH (WL), PIN DEMAND (PD) AND ROUTING DEMAND (RD) ARE REPORTED. RUNTIME IS IN SECONDS.

	best wirelength			2PIN_ASSIGN		
ckts	wl	pd	rd	wl	pd	rd
n10	1.0	11	15	1.2	9	11
n30	4.2	16	47	5.4	12	18
n50	8.6	31	70	12.0	15	59
n100	15.5	20	83	19.4	12	42
n200	34.3	23	139	42.4	11	76
n300	56.1	27	162	69.2	11	79
gt50	1.1	1010	3454	1.8	840	3111
gt100	2.3	1146	4468	4.1	1088	3507
gt300	4.3	882	6684	10.0	820	6542
gt1000	6.7	838	6310	28.7	760	10470
gt1500	8.3	913	9177	37.4	633	14165
TIME	2080			2638		

In the case of the gt benchmark, we notice that the violation for the best wirelength case is a lot more than the GSRC circuits. The wirelength is many times more than the best wirelength case because the circuits have much more nets than the corresponding GSRC circuits. The wirelength reported for the gt circuits are scaled to facilitate easier comparison. The parameters of the cost function are same as that used for the GSRC case. However the results show the same trends as the GSRC benchmarks.

B. Pin Assignment Results

In Table III we report the wirelength achieved during pin assignment. The result of the channel assignment is used as input to the pin assignment. For generating the best wirelength, we used the corresponding best wirelength channel capacities violating channel assignment. For the best wirelength, we allowed pin assignment algorithm to select routes without considering the pin assignment and routing demands. Our algorithm tries to minimize wirelength while avoiding congestion of routing channels and pin assignment

resources. The parameters of the algorithm decide the tradeoff between wirelength, pin assignment demands and routing demands. From our experiments we observe the following for the standard GSRC circuits:

- We are able to reduce pin demand and routing demand drastically at the cost of 25% increase in wirelength.
- The wirelength scales rapidly with benchmark sizes and the wirelength for pin assignment is huge compared to channel assignment due to limited routing resources in the floorplan layer.

The parameters of the pin assignment cost function was kept the same for all the gt benchmark and was the same as the one used for the GSRC benchmarks. Since there was a lot of violations in the best wirelength case for channel assignment, we derived the best wirelength case by using the channel assignment results produced by our algorithm. We notice that the the maximum pin assignment demands decreases for all the gt circuits while the bigger circuits show an increase in maximum routing demands, with many times increase in the wirelength. This suggests that by using different parameters for the cost function, we obtain tradeoff points among the pin demand, routing demand, and wirelength.

V. Conclusion

In this paper, we presented the channel and pin assignment algorithms for 3D packaging routing, which constitutes the final steps in our proposed routing flow for 3D packaging. The purpose of SOP channel assignment was to finish the connection between a pair of floorplan and pin distribution layers. We performed pin assignment in case the pin location of some blocks in floorplan layer is not determined. Our related experimental results demonstrate the effectiveness of our algorithm. This work completes our recently proposed global routing flow for 3D packaging. To the best of our knowledge, this work is the first to address channel/pin assignment in routing for 3D packaging.

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