# Multi-layer Floorplanning for Reliable System-on-Package

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**Abstract - Physical design automation for the new emerging mixed-signal System-on-Package (SOP) technology requires a new kind of floorplanner—it must place both active components such as digital IC, analog ICs, memory modules, MEMS, and opto-electronic modules, and embedded passive components such as capacitors, resistors, and inductors in a multi-layer packaging substrate while considering various signal integrity issues. We propose a new interconnect-centric multi-layer floorplanner named MF-SOP, which is based on a multiple objective stochastic Simulated Annealing method. The contribution of this work is first to formulate this new kind of floorplanning problem and then to develop an effective algorithm that handles various design constraints unique to SOP. The related experiments show that the area reduction of MF-SOP compared to its 2-D counterpart is on the order of $O(k)$ and wirelength reduction is 48% average for $k$-layer SOP, while satisfying design constraints.**

## I. INTRODUCTION

The next generation electronic packaging technology called System-on-Package (SOP) [1,2] integrates both active components such as digital IC, analog ICs, memory modules, MEMS, and opto-electronic modules, and embedded passive components such as capacitors, resistors, and inductors all into a single high speed/density multi-layer packaging substrate. SOP is more advanced than PCB, MCM [3], or SIP (System-in-Package) [4] since MCM handles the integration of digital ICs only and SIP handles digital components and passive elements only. Figure 1 shows the heterogeneous components integrated into the multi-layer substrate of System-on-Package. Moreover, the SOP design paradigm facilitates rapid reengineering via reuse libraries. Therefore, SOP promises a high return on investment at a very low risk within shorter time-to-market cycle compared to the System-On-Chip (SOC) paradigm.

A high performance mixed signal system employs a lot of passive components—up to 30 passive components per an IC. For example, Sony Handy Cam DCR-PC7 has 43 ICs and 1329 passive elements. Such passive components continue to take up much circuit board real estate. Therefore, rigorous attempts have been made to replaces them with so-called embedded passive components (EPC), which are small and flat enough to be inserted between package layers. EPCs allow devices to get smaller or designers to fit more functionality in the same space; eliminate the costs currently needed to purchase and solder on discrete devices; allow for more design flexibility; and derive electrical benefits from the different current path that would be traveled.

EPCs can also be used for simultaneous switching noise reduction, cross talk reduction, network matching, and signal integrity. The complexity of a radio frequency front-end IC is considerably simpler with high quality passive components. However, EPC placement needs to be done carefully while considering design constraints. First, the quality and functionality of RF circuits is extremely sensitive to any unforeseen parasitic. Thus, making interconnect as short as possible reduces parasitic and thus helps the performance and quality of radio frequency (RF) SOP. Second, decoupling capacitors perform well when they are close to the source of simultaneous switching noise. Hence, high performance mixed-signal systems benefit from close vicinity capacitors,



(a) digital IC with passives   (b) analog IC with passives   (c) Opto & memory components
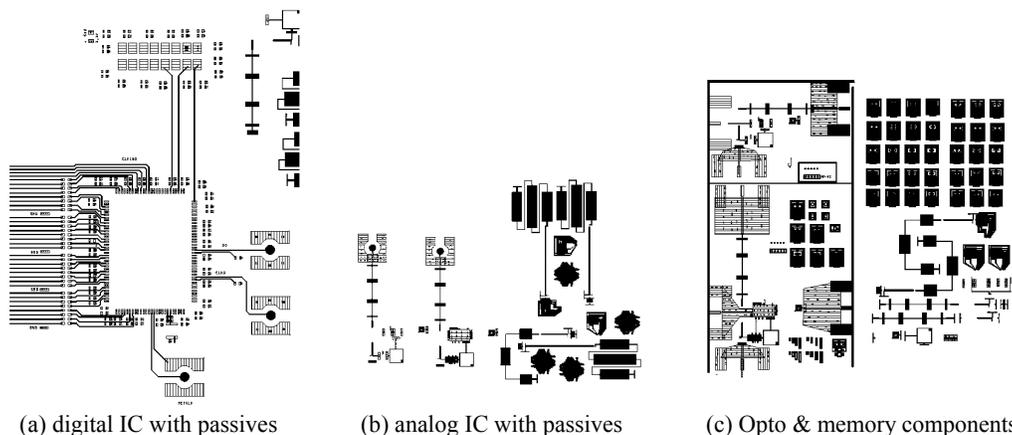
Figure 1 Mixed signal components integrated into multi-layer substrate of System-on-Package (courtesy of Packaging Research Center at Georgia Institute of Technology). (a) digital IC with its passive elements (only the footprint of a bare digital die is shown), (b) analog IC with its passive elements, and (c) opto-electronic and memory components with their passives. The passive elements are implemented in the active component layer for illustrative purpose. Some interconnections are not shown for simplicity.

which effectively stabilize supply and ground noise.

The physical layout resource environment of SOP is multi-layer in nature—the top layer is mainly used to accommodate active components, the middle layers are mainly for passive components, and the I/O pins are located at the bottom of the SOP package. Therefore, all layers are used for both placement and routing unlike PCB or MCM. Therefore, the existing design tools for PCB or MCM can not be used directly for the design of SOP. The existing work on multi-layer floorplanning is very few. Authors in [5] solved multi-layer floorplanning for vertically stacked digital systems. However, this work does not address the mixed-signal integration issues existing in SOP technology. Therefore, SOP technology requires a new kind of multi-layer floorplanner—it must place both active components and passive components in a multi-layer packaging substrate while considering various signal integrity issues. We propose a new interconnect-centric multi-layer floorplanner named MF-SOP, which is based on a multiple objective stochastic Simulated Annealing method. The contribution of this work is first to formulate this new kind of floorplanning problem and then to develop an effective algorithm that handles various design constraints unique to SOP. The related experiments show that the area reduction of MF-SOP compared to its 2-D counterpart is on the order of $O(k)$ and wirelength reduction is 48% average for k-layer SOP, while satisfying design constraints.

This paper organization is as follows. The problem formulation is given in Section II. SOP constraints are described in Section III. Experimental results and conclusions are given in Section IV and V, respectively.
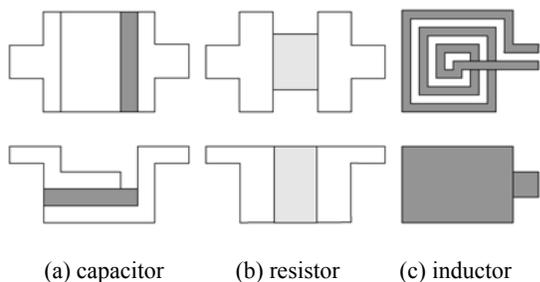


<div align="center">(a) capacitor   (b) resistor   (c) inductor</div>

Figure 2 Embedded passive components. Top and side views of typical RLC shapes are shown.

## II. PROBLEM FORMULATION

### A. Blocks in SOP Floorplanning

The major difference between 2-dimensional IC floorplanning and multi-layer SOP floorplanning lies in addressing the following issues related to the blocks to be floorplanned:

1. size/shape of the active and passive blocks
2. restrictions on block placement into certain layers (= *layer constraint*)
3. geometric constraints among active blocks (= *geometric constraint*)
4. geometric constraints between active and passive blocks (= *geometric constraint*)

First, most of the active components in SOP including digital IC, analog IC, memory module, opto-electronic modules, and MEMS have rectangular shape. Their area lies in a range of $[mm^2, cm^2]$. Figure 2 shows the shape of typical EPCs (embedded passive components). We assume rectangular shape for these EPCs. Their area lies in a range of $[\mu m^2, mm^2]$. Since both active and passive components have rigid shape, we do not consider "soft blocks" in our floorplanning. Second, most of the active components are required to be placed on the top layer due to heat dissipation requirement. However, some active components that do not generate too much heat can be placed in the middle layers. EPCs can be placed at any layers, but using middle layers is the most beneficial in reducing the overall footprint area of SOP. However, some EPCs are required to be placed on the top layer due to thermal and/or noise issues. Third, some active components need to be placed nearby together or apart from each other due to several reasons including signal/power integrity, performance optimization, etc. Lastly, most EPCs need to be placed closer to the related active components. Handling the layer constraints is straightforward, but the geometric constraints are harder to satisfy. Section III discusses in detail how to deal with these geometric constraints in our multi-layer SOP floorplanner.

### B. Problem Definition

A multi-layer SOP floorplan consists of a set $B=\{b_i| \ 0 \leq i < n\}$ of $n$ blocks and a set $L=\{l_i| \ 0 \leq i < k\}$ of $k$ layers. A block is either an active component or embedded passive component (EPC). We assume rectangular shape for all these blocks. Each floorplan $f_i$ has a set of blocks $B_i$, which is a non-empty proper subset of $B$. A SOP floorplan $F$ is represented by a set $F = \{f_0, f_1, ..., f_{k-1}\}$, where a floorplan $f_i$ is a 2-dimensional placement of blocks in $B_i$. In other words, $f_i = \{(x_j, y_j)| \ 0 \leq j < n(l_i)\}$, where $n(l_i)$ is the number of blocks in layer $l_i$ and $(x_j, y_j)$ is the coordinate of the lower left corner of block $b_j$. A SOP floorplan $F$ is *feasible* if (i) $F$ is free of overlap among block location, (ii) $F$ satisfies the layer and geometric constraints specified by the user. The width, height, and area of block $b_i$ are denoted $w(b_i)$, $h(b_i)$, and $a(b_i)$, respectively. Similarly, those of a floorplan $f_i$ and SOP floorplan $F$ are denoted $w(f_i)$, $h(f_i)$, $a(f_i)$, $w(F)$, $h(F)$, and $area(F)$. $w(f_i)$ and $h(f_i)$ are the width and height of the minimum size rectangle that contains all blocks in $f_i$, which can be computed by longest path length calculation [6]. $a(f_i)$ is $w(f_i) \times h(f_i)$. $w(F)$ is the maximum among all $w(f_i)$, and $h(F)$ is the maximum among all $h(f_i)$. $area(F)$ is $w(F) \times h(F)$.

Among many proposed methods to represent 2-dimensional floorplanning, we extend the sequence pair (SP) [7] to represent the multi-layer SOP floorplan solution. Our multi-layer sequence pair is represented by $(SP_0|SP_1|...|SP_{k-1})$, where $SP_i$ contains the positive and negative sequence for the blocks contained in layer $i$. In [5], the authors use BSG [8] structure to represent multi-layer floorplan. However, BSG has larger solution space with lots of redundancy. O-tree

[9]or B*-tree [10] can be extended for multi-layer floorplan and has a smaller solution space than both BSG and SP. However, SP requires a simpler perturbation implementation than O-tree or B*-tree. Thus, we choose SP as our multi-layer SOP floorplan solution representation. For a faster area evaluation for a given multi-layer SP, we use longest common subsequences (LCS) [6] method. A recent effort [11,12,13] uses various floorplanning representations to impose design constraints for 2-dimensional constraints.

Authors in [7] propose three types of moves for solution perturbation during Simulated Annealing: M1 (swap two modules in positive sequence), M2 (swap two modules from both positive and negative sequence), and M3 (rotate). We add two moves M4 and M5 to search the solution of multi-layer floorplanning effectively: M4 is similar to M3, except that the two blocks are from positive sequences in different layers. M5 selects a block from layer $i$ and moves it to another layer $j$. The location in positive and negative sequence from $SP_j$ is again randomly chosen.

*C. Cost Function*
We use the following cost function to measure the quality of an SOP floorplan solution $F$.

$$C(F) = c_1 area(F) + c_2 wire(F) + c_3 via(F) + c_4 penalty(F)$$

where $area(F)$, $wire(F)$, $via(F)$, and $penalty(F)$ respectively denote the area, wirelength, total number of vias, and the penalty related to constraint violation for $F$. The first term $area(F)$ is the final footprint area of SOP package, where $area(F) = w(F) \times h(F)$. The minimization of this objective results in a minimal overall SOP package area. The second term $wire(F)$ is the half-perimeter bounding box (HPBB) based estimation of wirelength. We ignore the height (z-dimension) of the *bounding cube* and use only the $x$ and $y$-dimension for the computation of the wirelength of a net. Instead, the z-dimension has a direct impact on $via(F)$. If a net $n$ spans from layer $i$ to layer $j$, then $via(n) = |i - j|$. The sum of $via(n)$ for all nets is $via(F)$. Our following Section III discusses in detail how $penalty(F)$ is computed. $penalty(F) = 0$ when there is no constraint violation in $F$.

We observe from related experiments that adding the following components to $C(F)$ results in a more compact multi-layer floorplan: *total flatten area flat(F)* and *dimension deviation dev(F)*. $flat(F)$ is the sum of all floorplans, $flat(F) = \sum a(f_i)$. The minimization of this objective results in a highly compact floorplan for each layer. $dev(F)$ measures how much the upper right corner (URC) of a floorplan deviates from the average URC. We compute the average URC ($u_x$, $u_y$) by $u_x = \sum u_x(f_i)/k$, where $u_x(f_i)$ denotes the x-coordinate of the URC of a floorplan $f_i$. We compute $u_y(f_i)$ using y-coordinates instead. Let $d(f_i) = |u_x - u_x(f_i)| + |u_y - u_y(f_i)|$ be the dimension deviation of a floorplan of $f_i$. Then $dev(F)$, the dimension deviation of SOP floorplan $F$ is simply the sum of all $d(f_i)$. The minimization of this objective results in a more dimension-balanced floorplan among all layers. It may seem redundant to have all three area-related objectives $area(F)$, $flat(F)$, and $dev(F)$ in $C(F)$. However, our related experiments indicate that each of these three objectives contribute to the minimization of not only the final footprint area $area(F)$ but

also the wirelength estimation $wire(F)$.

TABLE I. Geometric Constraints for SOP Floorplanning

| type | method | syntax | meaning |
|---|---|---|---|
| noise | point | $[b_i|(x,y,z)]$ | $b_i$ touches $(x,y,z)$ |
| thermal | layer | $[B_i|l]$ | $B_i$ in layer $l$ |
| power | region | $[B_i|(x,y,w,h)]$ | $B_i$ intersects with region $(x,y)$ and $(x+w,y+h)$ |
| timing | abutment | $[B_i]$ | $B_i$ abutted |
| interface | boundary | $[B_i|TBLR/l]$ | $B_i$ near boundary of layer $l$ |
| cluster | group | $[B_i|(x,y,z)]$ | $B_i$ within a distance of $(x,y,z)$ |

## III. GEOMETRIC CONSTRAINTS FOR MULTI-LAYER SOP FLOORPLANNING

*A. SOP Geometric Constraints*
We categorize the geometric constraints among active and passive components introduced in Section II.A into the following 6 types:
1. *noise*: decoupling capacitors are placed nearby I/Os or active components
2. *thermal*: some active/passive components are placed in certain layers
3. *power*: digital and analog ICs are placed in different voltage islands
4. *timing*: blocks from a critical path are placed closer
5. *interface*: I/O blocks are placed near the bottom layer
6. *cluster*: functionally dependant blocks are placed close together

Table I describes these 6 geometric constraint types we consider in SOP floorplanning. A prior timing analysis or signal integrity analysis is performed by the user[1] to identify (i) the source of timing, noise, thermal, and power supply problem, and (ii) ways to fix these problems in a form of constraint. Each constraint is then translated into a geometric form so that our multi-level floorplanner attempts to satisfy this geometric constraint. Our strategy is to quantify the amount of violation of the constraints specified, and guide Simulated Annealing-based optimization so that the amount of violation is minimized or completely removed if possible.

Our strategy for effective solution space search during Simulated Annealing is as follows:
1. construction of initial solution: we first assign all blocks under layer constraints to the target layers and fix them during the annealing. For the remaining blocks, we randomly and evenly distribute them into

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[1] We assume in this paper that the geometric constraints are specified by the user as an input to our multi-layer SOP floorplanner. The related timing and signal integrity analysis are time-consuming, and our ongoing research effort attempts to integrate STA (Static Timing Analysis), SIA (Signal Integrity Analysis), and TPA (Thermal and Power Analysis) engines into our floorplanner so that the geometric constraints are also automatically generated.

all layers.

2. solution perturbation: we perform more inter-layer moves (M4 and M5 discussed in Section II.A) during high temperature annealing and more intra-layer moves (M1, M2, and M3) during low temperature annealing.

3. weighting constants in $C(F)$: we focus more on penalty($F$) and via($F$) during high temperature annealing and more on area($F$) and wire($F$) during low temperature annealing.
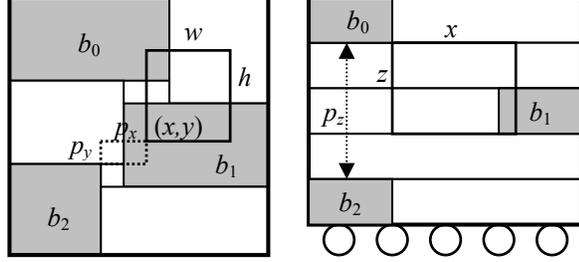


Figure 3 Constraint Examples. (a) region constraint $r_1=[\{b_0,b_4\}|(x,y,w,h)]$ and $r_2=[\{b_3,b_4\}|(x,y,w,h)]$. $r_1$ is satisfied and $r_2$ has penalty of $p_x+p_y$. (b) group constraint $g_1=[\{b_0,b_2\}|(x,y,z)]$ and $g_2=[\{b_0,b_7\}|(x,y,z)]$. $g_1$ is satisfied and $g_2$ has penalty of $p_z$. $y$-dimension is not shown.

### B. Illustration of SOP Geometric Constraint

An example of region constraint is given in Figure 3(a). First, consider $r_1=[\{b_0,b_1\}|(x,y,w,h)]$. Since both $b_0$ and $b_1$ are intersecting with the region defined by $(x,y,w,h)$, we see that $r_1$ is satisfied and the penalty is zero. Now consider $r_2=[\{b_1,b_2\}|(x,y,w,h)]$. Since $b_2$ is completely outside the region, $r_2$ is not satisfied and its penalty is computed by the sum of $p_x$ and $p_y$. An example of group constraint is given in Figure 3(b). First, consider $g_1=[\{b_0,b_1\}|(x,y,z)]$. Since the distance between $b_0$ and $b_1$ is within the 3-dimensional distance $(x,y,z)$, we see that $g_1$ is satisfied and the penalty is zero. Now consider $g_2=[\{b_0,b_2\}|(x,y,z)]$. Since the $z$-distance between $b_0$ and $b_2$ is bigger than $z$, $g_2$ is not satisfied and its penalty is $p_z$.

TABLE II. Penalty Computation for $x$-dimension ($p_x$). Penalty for $y$ ($p_y$) and $z$ ($p_z$) dimensions can be computed similarly using $y$/$z$-coordinates and height/layer information. The overall penalty $p= p_x+ p_y+ p_z$.

| method | syntax | penalty ($p_x$) |
|---|---|---|
| point | $p=[b_i|(x,y,z)]$ | $\min\{|x-x_i|, |x-(x_i+w_i)|\}$ |
| layer | $l=[B_i|l]$ | $\sum|l(b_i)-l|$ |
| region | $r=[B_i|(x,y,w,h)]$ | $\sum\min\{|x-(x_i+w_i)|, |(x+w)-x_i)|\}$ |
| abutment | $a=[B_i]$ | $\sum[(x_i+w_i)-x_j]$, $b_i$ and $b_j$ separated |
| boundary | $b=[B_i|TBLR/l]$ | $\sum[w(f_i)-(x_i+w_i)]$ for R boundary |
| group | $g=[B_i|(x,y,z)]$ | $\sum[x-|(x_i+w_i)-x_j|]$, if $|(x_i+w_i)-x_j|> x$ |

### C. Penalty Computation

The penalty computation for constraint violation is summarized in Table II. Penalty computation for $x$-dimension ($p_x$) is shown only, but other dimensions ($p_y$) and ($p_z$) can be computed similarly using $y$/$z$-coordinates and height/layer information. The overall penalty $p=p_x+ p_y+ p_z$. Note that $p_z$ contributes to our via cost and usually carries more weights than $p_x$ or $p_y$. The point, layer, and region constraints are *intersection-based*—these constraints are violated if there is no intersection between the blocks and the region given. The abutment, boundary, and group constraints are *distance-based*—these constraints are violated if the distance among the blocks is bigger than the given threshold. We specify absolute coordinates for the intersection-based constraints, whereas relative distance information is given in distance-based constraints. Finally, the overall penalty function *penalty($F$)* for a given SOP floorplanning solution $F$ is the sum of the penalty among all constraints given.



(a) 4-level SOP    (b) top-view    (c) layer 0

(d) layer 1    (e) layer 2    (f) layer 3
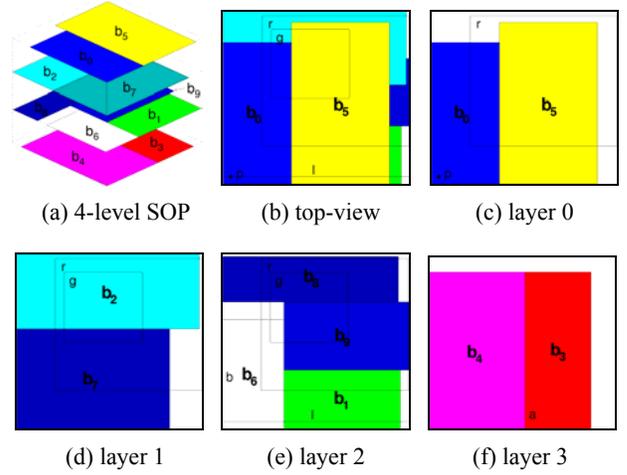
Figure 4. A 4-layer SOP floorplanning with 10 blocks with the following 6 geometric constraints: $p=[b_0|(10,10,3)]$, $l=[\{b_1\}|0]$, $r=[\{b_2\}|(3,3,5,5)]$, $a=[\{b_3,b_4\}]$, $b=[\{b_6\}|L]$, $g=[\{b_7,b_8\}|(5,5,5)]$.

In an example shown in Figure 4, we use the following 6 constraints for 4-layer SOP floorplanning with 10 blocks: $p=[b_0|(10,10,3)]$, $l=[\{b_1\}|0]$, $r=[\{b_2\}|(3,3,5,5)]$, $a=[\{b_3,b_4\}]$, $b=[\{b_6\}|L]$, $g=[\{b_7,b_8\}|(5,5,5)]$. This example considers all six types of SOP constraints given in Table I. Figure 4 shows a solution $F$ that includes several constraint violations. In the top layer (layer 0) we have two active components $b_0$ and $b_5$ while other layers contain embedded passive components. First, the point constraint $p=[b_0|(10,10,3)]$ is not satisfied in $F$ since $b_0$ is in layer 0 instead of layer 3 although $b_0$ contains the point (10,10) in $x$/$y$ dimension. This increases the via cost by 3. Second, the layer constraint $l=[\{b_1\}|0]$ is not satisfied since $b_1$ is in layer 2 instead of layer 0. This also increases the via cost by 2. Third, the region constrain $r=[\{b_2\}|(3,3,5,5)]$ is satisfied in $F$ since $b_2$ intersects with the given region (= rectangle labeled $r$). Thus the penalty is zero. Fourth, the abutment constraint $a=[\{b_3,b_4\}]$ is satisfied in $F$ since $b_3$ and $b_4$ in layer 3 are abutted. Thus the penalty is zero. Fifth, the boundary constraint $b=[\{b_6\}|L]$ is satisfied in $F$ since $b_6$ is in

contact with the left boundary of layer 2. Thus the penalty is zero. Lastly, the group constraint $g=[\{b_7,b_8\}|(5,5,5)]$ is satisfied in $F$ since the distance between $b_7$ and $b_8$ in all three dimension is smaller than the size of the given cube (= rectangle labeled $g$). Thus the penalty is zero.

## IV. EXPERIMENTAL RESULTS

We implemented our algorithm MF-SOP in C++/STL and ran on a Dell Dimension 8800 Linux box. We used GSRC floorplanning benchmark circuits. We report the area, wirelength, inter-layer via, and runtime for 4-layer SOP in all of our experiments. Figure 5 shows 4-layer SOP floorplanning for n100 (GSRC benchmark circuit). Table III shows the comparison among (i) single-layer floorplanning, (ii) 4-layer SOP floorplanning without geometric constraints, and (iii) 4-layer SOP floorplanning with geometric constraints. We summarize our observations here:

1. compared to the single layer floorplanning, the final package area for 4-layer floorplanning is reduced by 75% on the average (order of $O(k)$ reduction). This indicates that the floorplan for all 4 layers is highly compact and their shapes are similar. The impact of geometric constraint on final area was not significant—79800 vs 81354. This shows the effectiveness our MF-SOP in obtaining high quality multi-layer SOP floorplanning solutions in the presence of complex design constraints in SOP.
2. the wirelength reduction for 4-layer floorplanning is 40% on the average compared to the single-layer case. Since the wirelength in $z$-direction is not considered (this is actually our via cost), the 40% saving mainly comes from the final package area reduction. The impact of geometric constraint on final wirelength was not significant—418560 vs 422960.
3. The impact of geometric constraint on via results was not significant—1953 vs 1893. In some cases MF-SOP was able to find a solution with smaller wirelength and via. This again shows the effectiveness our MF-SOP in handling complex design constraints in SOP.
4. The runtime has been increased by 10x with 4-layer floorplanning. The runtime slightly increased when MF-SOP considers geometric constraints. There are several factors that contribute to the runtime increase: (i) we need highly compact floorplan for all 4 layers and their shapes need to be similar, (ii) we need to minimize 2-dimensional wirelength and via cost simultaneously.

Table IV shows the total number of initial and final constraints used in Table III. We also report the number of failed constraints for each constraint type in each circuit. We randomly select constraints from 6 types for each circuit, and we impose more constraints for bigger circuits. We summarize our observations here:

1. We observe that abutment ($a$), boundary ($b$), and group ($g$) constraints are easier to satisfy than point ($p$), layer ($l$), and region ($r$) constraints. We note that the

distance-based constraints are easier to handle than the intersection-based constraints. This indicates that specifying the absolute location is a stronger constraint rather than the relative distance.
2. Point constraint was the hardest to satisfy, followed by boundary constraint. Layer constraint is always satisfied since our initial solution satisfy the layer constraint before Simulated Annealing, and we lock all blocks under layer constraints and do not move.

Table IV. Total number of initial and final constraints used in Table III. We also report the number of failed constraints for each constraint type.

| | # of constraints | | failed constraint types | | | | | |
|---|---|---|---|---|---|---|---|---|
| ckts | initial | final | $p$ | $l$ | $r$ | $a$ | $b$ | $g$ |
| n10 | 6 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| n10b | 6 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| n10c | 6 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| n30 | 10 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| n30b | 10 | 5 | 1 | 0 | 2 | 0 | 2 | 0 |
| n30c | 10 | 3 | 1 | 0 | 1 | 0 | 1 | 0 |
| n50 | 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| n50b | 12 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| n50c | 12 | 3 | 1 | 0 | 0 | 0 | 1 | 1 |
| n100 | 14 | 2 | 1 | 0 | 0 | 0 | 1 | 0 |
| n100b | 14 | 4 | 2 | 0 | 1 | 0 | 1 | 0 |
| n100c | 14 | 3 | 2 | 0 | 0 | 0 | 1 | 0 |
| n200 | 14 | 2 | 2 | 0 | 0 | 0 | 0 | 0 |
| n200b | 14 | 3 | 2 | 0 | 0 | 0 | 1 | 0 |
| n200c | 14 | 2 | 2 | 0 | 0 | 0 | 0 | 0 |
| n300 | 14 | 2 | 2 | 0 | 0 | 0 | 0 | 0 |
| total | 182 | 34 | 21 | 0 | 4 | 0 | 8 | 1 |

## V. CONCLUSIONS

In this paper, we proposed a new multi-layer floorplanner MF-SOP for the new emerging mixed-signal System-on-Package (SOP) technology. MF-SOP places both active components such as digital IC, analog ICs, memory modules, MEMS, and opto-electronic modules, and embedded passive components such as capacitors, resistors, and inductors in a multi-layer SOP substrate. MF-SOP considers 6 types of geometric constraints in order to address various signal, thermal, and power integrity issues existing in the design of reliable SOP. Our ongoing research effort attempts to integrate STA (Static Timing Analysis), SIA (Signal Integrity Analysis), and TPA (Thermal and Power Analysis) engines into our floorplanner so that the geometric constraints are also automatically generated. The goal is to develop built-in STA/SIA/TPA that runs fast but with high fidelity so that they will not slow down the optimization process while guiding the optimization for high quality multi-layer SOP floorplanning solution.

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Table III. Comparison among (i) single-layer floorplanning, (ii) 4-layer SOP floorplanning without geometric constraints, and (iii) 4-layer SOP floorplanning with geometric constraints. We report the package area, wirelength, total number of vias used, and total runtime. Table IV shows the type of constraints used in this experiment.

| | $k$=1 | | $k$=4, no constraint | | | $k$=4, constraint | | |
|---|---|---|---|---|---|---|---|---|
| | area | wire | area | wire | via | area | wire | via |
| n10 | 258152 | 18164 | 98000 | 8693 | 118 | 73738 | 6209 | 118 |
| n10b | 251778 | 15128 | 94912 | 7309 | 133 | 78690 | 6252 | 133 |
| n10c | 268865 | 19880 | 125928 | 11720 | 119 | 70596 | 6397 | 119 |
| n30 | 245115 | 54586 | 75749 | 27288 | 349 | 66505 | 23830 | 349 |
| n30b | 234574 | 45931 | 67670 | 23674 | 350 | 56156 | 20248 | 350 |
| n30c | 233867 | 55979 | 88795 | 24259 | 390 | 71638 | 24166 | 390 |
| n50 | 231431 | 104395 | 64829 | 59411 | 485 | 61254 | 49463 | 485 |
| n50b | 237266 | 94790 | 67130 | 56629 | 511 | 72500 | 46726 | 511 |
| n50c | 234567 | 106562 | 59823 | 58182 | 515 | 62160 | 53446 | 515 |
| n100 | 210378 | 180413 | 55081 | 117407 | 885 | 53320 | 105350 | 885 |
| n100b | 185868 | 169767 | 49608 | 100657 | 806 | 52425 | 101895 | 806 |
| n100c | 208616 | 185215 | 54273 | 109932 | 852 | 52974 | 109925 | 855 |
| n200 | 214349 | 393644 | 55722 | 251626 | 1585 | 56810 | 260678 | 1585 |
| n200b | 208960 | 336236 | 53799 | 240673 | 1714 | 54707 | 235781 | 1714 |
| n300 | 206954 | 394358 | 51684 | 262042 | 1532 | 52416 | 255327 | 1585 |
| ave | 329589 | 658162 | 79800 | 418560 | 1953 | 81354 | 422960 | 1893 |
| ratio | 1.00 | 1.00 | 0.24 | 0.64 | 1.00 | 0.25 | 0.64 | 0.97 |
| runtime | 132 | | 1070 | | | 1109 | | |



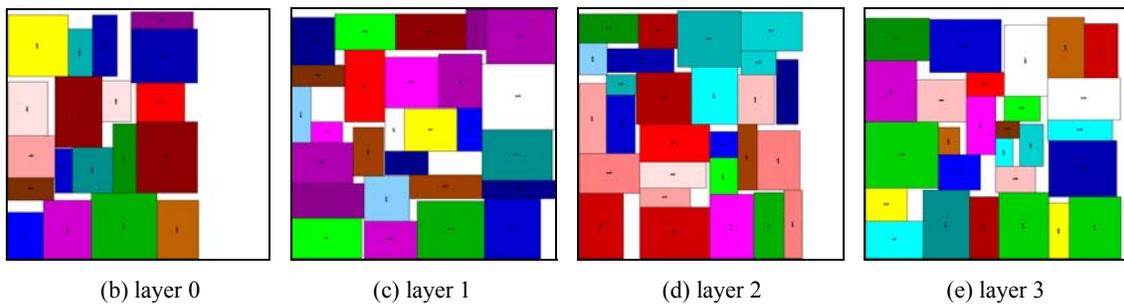(b) layer 0        (c) layer 1        (d) layer 2        (e) layer 3

Figure 5. 4-layer SOP floorplanning for n100 (GSRC benchmark circuit).