The IBM Power Edge of Network™ Processor:
A wire-speed System-on-a-Chip with 16 Power™ cores / 64 threads and optimized HW acceleration

Hubertus Franke
Research Staff Member, Mgr Scalable Systems Department
IBM T.J. Research Center
Yorktown Heights, NY 10598
frankeh@us.ibm.com

Co-authors: To many to mention (Research / STG)
Chief Architects: Charlie Johnson, Jeff Brown
Disruptive Innovations

- Cloud Computing
- Smarter Planet
- SOA
- Virtual Worlds
- Mashups
- Crowdsourcing
- Software as a Service
- Web 2.0
- Petaflop Supercomputers
- Game Players
- Mobile Devices
- Globally Integrated Enterprise
- Services Sciences
- Physics
- Mobile Devices Crowdsourcing

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Reinventing How Systems are Built

- Technology discontinuities driven by physics
- Business needs driving specialized hybrid systems
- Hybrid system future directions
Key Technology Inflection Points

<table>
<thead>
<tr>
<th>Bipolar to CMOS Transition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
</tr>
<tr>
<td>Density</td>
</tr>
<tr>
<td>Transistor Speed</td>
</tr>
</tbody>
</table>

Massively multi-threaded (parallel) architectures + accelerators
Microprocessor Technology Trends

- **Chip Power**: Watts
  - Practical power limit

- **Single Thread Performance**: SPECint
  - Single thread perf growth rate slows

- **Chip Power Efficiency**: SPECint_rate per Watt
  - 8 Core, 4 Core, 2 Core, 1 Core
Future Systems and New Applications

- Emerging applications for richer data formats and near real-time sources of data

- Security, analytics, and application acceleration are key
Future Systems and New Applications

- Emerging applications will require substantial improvements in system characteristics

- New purpose-optimized computational elements will fundamentally transform systems
Opportunity Exists for Optimization Across the Workload Space

### System Workload Categorization

<table>
<thead>
<tr>
<th>Transaction Processing and Database</th>
<th>Business Process Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Data Warehousing</td>
<td>- ERP</td>
</tr>
<tr>
<td>- OLTP</td>
<td>- SCM</td>
</tr>
<tr>
<td>- Batch</td>
<td>- CRM</td>
</tr>
<tr>
<td>- Business Processing DB</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Analytics and High Performance Computing</th>
<th>Web, Collaboration and Infrastructure</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Data Mining Applications</td>
<td>- Application Development</td>
</tr>
<tr>
<td>- Numerical</td>
<td>- Systems Management</td>
</tr>
<tr>
<td>- Enterprise Search</td>
<td>- Infrastructure DB</td>
</tr>
<tr>
<td>- Gaming &amp; Visualization</td>
<td>- File &amp; Print</td>
</tr>
<tr>
<td></td>
<td>- Web/Collaboration Content DB</td>
</tr>
<tr>
<td></td>
<td>- Web Serving/Hosting</td>
</tr>
<tr>
<td></td>
<td>- Web/Networking Acceleration</td>
</tr>
<tr>
<td></td>
<td>- Security</td>
</tr>
<tr>
<td></td>
<td>- Networking</td>
</tr>
<tr>
<td></td>
<td>- IMS/VOIP Infrastructure</td>
</tr>
<tr>
<td></td>
<td>- Proxy Caching</td>
</tr>
<tr>
<td></td>
<td>- Collaboration</td>
</tr>
</tbody>
</table>

### Workload Attributes

<table>
<thead>
<tr>
<th>Transaction Processing and Database</th>
<th>Analytics and High Performance Computing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scale</td>
<td>Compute intensive</td>
</tr>
<tr>
<td>High Transaction Rates</td>
<td>High I/O Bandwidth</td>
</tr>
<tr>
<td>High Quality of Service</td>
<td>High Memory Bandwidth</td>
</tr>
<tr>
<td>Handle Peak Workloads</td>
<td>Floating point</td>
</tr>
<tr>
<td>Resiliency and Security</td>
<td>Scale-out Capable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Business Process Applications</th>
<th>Web, Collaboration and Infrastructure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scale</td>
<td>Highly Threaded</td>
</tr>
<tr>
<td>High Quality of Service</td>
<td>Throughput-oriented</td>
</tr>
<tr>
<td>Large Memory Footprint</td>
<td>Scale-out Capable</td>
</tr>
<tr>
<td>Responsive Infrastructure</td>
<td></td>
</tr>
</tbody>
</table>

**Scale-out Capable**
Wire-Speed Processing

A blurring of the **Network** and **Server** worlds

- Highly-multi-threaded low power cores with full PPC ISA
- Standard programming models with OS’s & hypervisors
- Virtualization support for application consolidation
- Accelerators: for both Networking & Application tiers
- Integrated Network system & Memory I/O
- Server RAS & infrastructure
- Low total power solution based on throughput optimization
Wire-speed Differentiated Solutions

Emerging class of throughput and latency sensitive applications whose performance and scaling require the optimization of both networking and computing on specialized wire-speed processors.

Applications require: near real-time latency, high throughput, and ability to scale 1-1 with networking roadmaps.

Examples: Deep-Packet Inspection (DPI) as prototypical transformation function for security, monitoring, filtering, pattern matching, and data conversions.

As data flow is transient for network-optimized applications, compute resources must process data and scale with networking rates with near real-time latency.

Systems require: a scalable wire-speed compute node as basis engine which cannot be accomplished with commodity components due to compute density, throughput, latency, and power requirements.

- Massively multi-threaded cores for concurrency, latency and power
- Accelerators for throughput, latency and power
- Tightly coupled integrated I/O for performance and latency

Pervasive wire-speed compute node forms the basis for a class of highly scalable and distributed computing and stream-based systems.
IBM PowerEN™: Targeted at the Edge-of-Network

- Power efficient Throughput computing
  - Database Acceleration
  - Service Oriented Architecture Acceleration
  - Secure Multi-tenant Cloud Computing
- Enhanced processing of data payloads
  - Low latency message for Financial Information Exchange
- Deeper networking functions
  - Cyber Security
  - Network Intrusion Prevention
- Application targeted at "smarter planet" solutions
  - Compartmentalized streamed analytics
  - Data Reduction in storage subsystems
Power EN Wire-speed processing system

**Massive Multi-Threading**
- High-efficiency design: Performance per watt & performance per cu. foot
- Simplicity of SMP programming model reduces S/W development costs

**Accelerators**
- Crypto for pervasive security
- Compression for BW opt.
- XML for SOA support
- Pattern matching for filtering

**Integrated I/O**
Efficient system-level I/O processing driven by emerging application requirements

**Network packet processing engine**

**I/O and Network Engines**

**Compute / Memory**

**Power/Perf Efficiency**
- Unique Accelerator
- MMT Processor
- General Purpose Processor

**SW complexity**
- 10 - 100X Improvement
- 2 - 4X Improvement

**4-chip SMP capability**
Overview of IBM PowerEN™ Processor Chip

- 64-bit PowerPC Architecture
- Virtualization Support
- Dual DDR3 DRAM Controllers
- Optimized Ethernet Offload Engine
- Integrated PCI-Express bus
- Cryptography Unit
- Regular Expression Unit
- XML Processing Unit
- Compression Unit
- Upward Scalability – 4 Chip
- Downward scalability - Subset

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**PowerEN™ has all basic IP needed for user/data plane and control plane traffic processing**
## PowerEN: Wire-Speed Processor

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>IBM 45nm SOI</td>
</tr>
<tr>
<td>Core Frequency</td>
<td>2.3GHz @ 0.97V (Worst Case Process)</td>
</tr>
<tr>
<td>Chip size</td>
<td>428 mm2 (including kerf)</td>
</tr>
<tr>
<td>Chip Power (4-AT node)</td>
<td>65W @ 2.0GHz, 0.85V Max Single Chip</td>
</tr>
<tr>
<td>Chip Power (1-AT node)</td>
<td>20W @ 1.4GHz, 0.77V Min Single Chip</td>
</tr>
<tr>
<td>Main Voltage (VDD)</td>
<td>0.7V to 1.1V</td>
</tr>
<tr>
<td>Metal Layers</td>
<td>11 Cu (3-1x, 2-1.3x, 3-2x, 1-4x, 2-10x)</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>1.43B</td>
</tr>
<tr>
<td>A2 Cores / Threads</td>
<td>16 / 64</td>
</tr>
<tr>
<td>L1 I &amp; D Cache</td>
<td>16 x (16KB + 16KB) SRAM</td>
</tr>
<tr>
<td>L2 Cache</td>
<td>4 x 2MB eDRAM</td>
</tr>
<tr>
<td>Hardware Accelerators</td>
<td>Crypto, Compression, RegX, XML</td>
</tr>
<tr>
<td>Intelligent Network Interfaces</td>
<td>Host Ethernet Adapter/Packet Processor 2 Modes: Endpoint &amp; Network</td>
</tr>
<tr>
<td>Memory Bandwidth</td>
<td>2x DDR3 controllers 4 Channels @ 800-1600MHz</td>
</tr>
<tr>
<td>System I/O Bandwidth</td>
<td>4x 10G Ethernet, 2x PCI Gen2</td>
</tr>
<tr>
<td>Chip-to-Chip Bandwidth</td>
<td>3 Links, 20GB/s per link</td>
</tr>
<tr>
<td>Chip Scaling</td>
<td>4 Chip SMP</td>
</tr>
<tr>
<td>Package</td>
<td>50mm FCPBGA (4 or 6 layers)</td>
</tr>
</tbody>
</table>

![PowerEN Microarchitecture Diagram](image-url)
### Special Purpose Hardware - PowerEN

#### Accelerator Bandwidths

<table>
<thead>
<tr>
<th>Accelerator Unit</th>
<th># of Engines</th>
<th>Algorithm</th>
<th>Typical Bandwidth</th>
<th>Peak Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>single stream</td>
<td>total</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>single stream</td>
<td>total</td>
</tr>
<tr>
<td><strong>HEA</strong></td>
<td>4</td>
<td>Network node mode (Gbps)</td>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>Endpoint mode (Gbps)</td>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td><strong>De/Compression</strong></td>
<td>1</td>
<td>Compression (Gbps input)</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Decompression (Gbps output)</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td><strong>Security Unit</strong></td>
<td>8</td>
<td>DES (Gbps)</td>
<td>4</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>AES (Gbps)</td>
<td>5</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>TDES (Gbps)</td>
<td>2</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>ARC4 (Gbps)</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Kasumi (Gbps)</td>
<td>2.5</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>SHA-1,256,512 (Gbps)</td>
<td>3.5 - 4</td>
<td>21 - 24</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>MD5 (Gbps)</td>
<td>4</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>AES/SHA-1,256,512 (Gbps)</td>
<td>2 - 3</td>
<td>10 - 15</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>TDES/SHA-1,256,512 (Gbps)</td>
<td>1.5 - 2</td>
<td>9 - 12</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>RSA/ECC exp. w/ 1024/2048 bits / key (ops / second)</td>
<td>15000 / 2000</td>
<td>45000 / 6000</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>(Gbps input)</td>
<td>2.5 - 5</td>
<td>20-40</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>(Gbps input)</td>
<td>1 - 3</td>
<td>4 - 12</td>
</tr>
</tbody>
</table>

*Multiple algorithms can be processed in parallel but aggregate bandwidth may be effected*
PowerEN:
Projected power breakdown by function @ 2.0GHz

- Cores/Caches: 40%
- Accelerators: 11%
- I/O & Bus Logic: 19%
- PHY: 27%
- Clock Grid: 3%
Evolution of a Wire-Speed Processor
Power Savings from Architecture / Integration

- Low Power Integrated Design
  -- Accelerators
  -- I/O (Ethernet/HEA)
  -- Cores/Threads
  -- In 25-75 W Sockets

1. Eliminates I/O Bottlenecks
2. Improves Latency & State Replication
3. Scalable Solution
   -- 10 => 40 => 100 GbE

[General Purpose Processor chip] 0: 8- GP cores
1: 8- GP cores + 4 Accelerators
2: 8- GP cores + 4 Accelerators + Integrated I/O (DDR3, 10Ge, HEA)
3: 16- A2 cores + 4 Accelerators + Integrated I/O (DDR3, 10Ge, HEA)

Wire Speed Processor Chip
Power-Performance Options @ 2.3GHz

Projected Power vs. Projected Relative Performance
(WirespeedBenchmark)

50% power reduction at constant performance

better
Interconnect Architecture

- **“All Peers” architecture**
  - Accel. and I/O are *first class citizens*
- Proven Power-Bus architecture
  - Independent CMD Network (one/cycle)
  - Two north, two south 16B data busses
  - ECC protected data paths
- 64 Byte Cache Line
- Cache Injection
  - Packets flow to / from Caches
  - New PBus commands:
- 1.75 GHz operation
  - Asynchronous connection to AT Nodes and accelerators via PBICs
  - Synchronous connection to DRAM controllers
  - Three 4B 2.5 GHz EI3 external links (1, 2, or 4 chip systems)
PowerPC™ Processing Element Architecture

- PowerPC 64 architecture – Embedded
- Enhanced for Co-processor/I/O interface
- 4 way Fine Grained SMT
- In Order Dispatch and Execution
- 2 way concurrent issue.
  - 1 Integer + 1 FPU instruction per cycle
  - Different threads
- Unified fixed point, ld/st, and branch unit
- 16KB L1 Data Cache – 4 Way Assoc.
- 16KB L1 Instr Cache – 8 Way Assoc.
- 12 Stage Pipe 27 FO4 design (7 XU, 5 IU, 6 FU)
- Fully associative I and D – ERAT
- MMU: 512 Entry TLB w/ Hardware Table Walk
- Hypervisor / Virtualization - One logical partition per core
PowerPC™ Processing Element Architecture

- 4 cores x 4 slices of shared L2
  - 512KB per slice
  - Concurrent reload data to all 4 cores
- 1:1 with processor cycle time
- 2MB eDRAM (total)
  - 64B cache lines
  - Inclusive of L1 I & D caches
  - 8 way set associative
- Fast core wake up on reservation loss
- ECC (SEC/DED) Data and on Directory
- Line locking & Way locking
- Slave memory region (non-coherent)
- Cache injection (full & partial line)
- Power Saving Mode: Rip Van Winkle
Two independent DDR3 DRAM controllers
- 2 independent channels / controller
- Registered RDIMMs or unbuffered UDIMMs
- Up to two DIMMs per channel and 1, 2 or 4 ranks on DIMM
- Attach up to 32 GB per DRAM controller
- 64 byte block ECC matches cacheline size
- 800 MHz, 1.066 GHz, 1.33 GHz, 1.6GHz DRAMS

PBus Interface
- One PBus interface (C/D) per controller
- Capable of 16 Bytes outbound per PBus cycle and 16 Bytes inbound per PBus cycle
Accelerator (Co-Processor) Architecture

- Objectives
  - Performance
  - Common API (Ease of Use)
  - QOS
  - Virtualization – Protection
- Common Architecture for all Accelerators
- Integrated in Power Architecture
  - New Initiate Co-Processor Instruction
  - New Wait on Loss of Reservation
    - (Thread wake up)
  - Application Context communicated to Co-Processor
  - Access Control
- L2 Cache Intervention / Injection
- Accelerator MMU derived from Processor MMU
  - Accelerators operate in Application Address Space
Accelerator Interface

1. Software receives an input packet
2. Software builds the CPB and CRB in cache
3. Software issues the ICSWX instruction
4. L2: ICSWX => Cop_Req PBus command
5. The PBus transports the Cop_Req
6. The PBIC passes the CRB and Cop_Req to Accelerator
7. The DMA logic assigns the Algorithm Engine and fetches data and parameters
8. The DMA logic and the Algorithm Engine work together to process the data and generate the output data
9. The DMA logic stores the output data
10. The DMA logic stores the status into the CSB
11. The DMA logic performs the final handshake
12. The SW retrieves the output status and data
Compression/Decompression

- **Standards**
  - Supports file formats defined by RFC1950 (ZLIB) and RFC1952 (GZIP)
  - Compliant to RFC1951 and DEFLAT

- **Pipelined data engine**
  - Deep pipelines to minimize latency and increase bandwidth
  - 8 Gbps output from engine (Decomp)
  - 8 Gbps input to engine (Comp)

- **Decompression**
  - Supports interleaved messages, packet by packet decompression
  - Static & Dynamic Huffman decoding supported

- **Compression**
  - Supports single messages to be compressed
  - Static Huffman coding support
Crypto Data Mover

- Symmetric Algorithm Acceleration
  - AES Modes:
    - Key Lengths: 128b, 192b, 256b
  - DES & 3DES Modes:
    - ARC4, Kasumi
  - HASH: SHA-1, SHA-256, SHA-512, MD5
    - HMAC supported for SHA
    - Combined 3DES/AES and SHA

- Asymmetric Algorithm Acceleration
  - Modular Math Functions for RSA/ECC
  - Point Functions for ECC
  - RSA lengths: 512b, 1024b, 2048b, 4096b

- Asynchronous Data Mover (ADM)
  - Any Source Byte offset, Any Dest Byte offset, Any length up to 16M bytes

- Random Number Generator (RNG)
  - Supplies a 64b random number, Supports FIPS 140 compliance
XML Unit / XML Engines

- Fully asynchronous offload operation
- Four Parsing Engines
  - Performs lexical analysis
  - Checks well-formness
  - Normalizes whitespace
  - Seamlessly switches state to process interleaved document fragments
  - Processes multiple characters simultaneously
  - Supports multiple character encodings
- Four Post Processing Engines
  - XPATH evaluation
  - Schema validation
  - Filtering in hardware (reject)
  - Process a fragment of incoming document
  - XSLT processing, XML Routing
RegX (Pattern Matching Engine)

- Processes 8 CRB’s in parallel
- Four independent Physical Lanes; each composed of 4 programming state machines (BFSM)
  - Each lane is time multiplex by two logical lanes
  - Each BFSM is connected to 32KB of SRAM (total of 512KB)
- SRAM holds resident rules (SW managed cache) and temporary rules (HW managed cache)
- Strong dependency between hardware, compiler, patterns and workload
IBM PowerEN™ Packet Processing Framework

Parallel Processing

Control Plane:
Call Set-up
Routing
Mobility
Management

Data Plane:
Bulk of Protocol Processing
Packet Forwarding
Packet Alteration
Egress Queue Selection

Centralized Processing

Packet Pre-Processor

Packet Post-Processor

Packet Classification
Filtering
Traffic management
Buffer management
Ingress Queue Selection
Thread Scheduling

Crypto – RegEx – XML
CompDecomp

Accelerators

Interconnect

Centralized Processing

Packet Ordering
Traffic management
Buffer management
Ingress Queue Selection
Thread Scheduling

Processing Element

Processing Element

Processing Element
Packet Processor Architecture

- Offload Centralized Media Speed Functions
  - Packet Classification /Distribution / Ordering
  - BFSM based Parser
  - Virtualization - Up to 16 LPARs, Integrated L2 virtual Switch, PVID
- END POINT MODE: L4+ termination
  - Pull model Software interface (128 Queues)
  - Scatter/gather descriptors
  - Low latency Queues, Header separation
  - TCP/UDP IPv4, v6 Checksum assist
  - QOS support (ingress Queue selection)
- NETWORK NODE MODE: Packet forwarding
  - Push model Software interface (64 Queues)
  - HW managed queues
  - Ingress – Egress Scheduler (Flexible ingress queue) selection
  - Completion Unit (Packet ordering – 16K packets)
  - Thread to Thread messaging with ordering
PCI-Express

- Two PCIe ports
- PCIe Gen 2 Features
  - 5Gb/sec per lane/direction
  - Max Payload: 512B, Max Read: 4K
- Root Port Mode - PHB
  - IODA-based definition
  - TCE based Address Translation
    - TCE cache: 64-entry 4-way
    - Inbound MSI Validation
- Endpoint Mode
  - PCIe SRIOV Virtualization
  - DMA Follows accel. SW model
    - Engaged via Coprocessor Request
    - Similar compl/status reporting
    - Tx and Rx data streaming engines
  - Separate Doorbell and Interrupts per PCIe PF/VF
  - Dedicated Mailbox space
IBM PowerEN™ Processor Chip

- Targeted at the Edge-of-network
- Power efficient Throughput computing
- Enhanced processing of data payloads
- Deeper networking functions
- Application targeted at "smarter planet" solutions

PowerEN™ has all basic IP needed for user/data plane and control plane traffic processing at the Edge of Network
Thank you